



VFC320

## Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

### FEATURES

- **HIGH LINEARITY**, 12 to 14 bits  
±0.005% max at 10kHz FS  
±0.03% max at 100kHz FS  
±0.1% typ at 1MHz FS
- **V/F OR F/V CONVERSION**
- **6-DECADE DYNAMIC RANGE**
- **20ppm/°C max GAIN DRIFT**
- **OUTPUT TTL/CMOS COMPATIBLE**

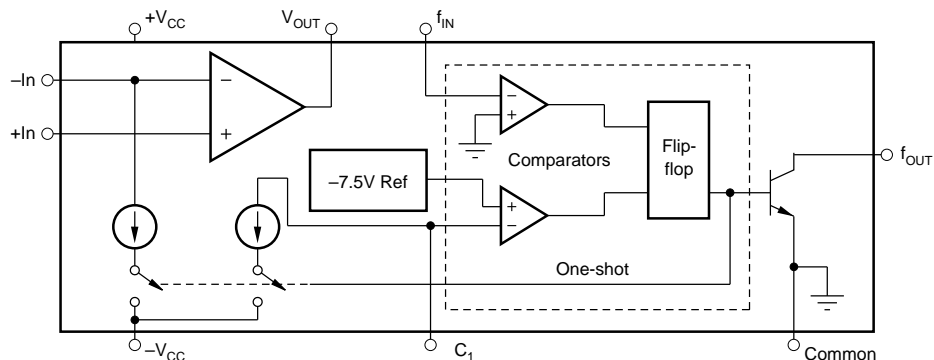
### APPLICATIONS

- **INEXPENSIVE A/D AND D/A CONVERTER**
- **DIGITAL PANEL METERS**
- **TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY**
- **FM MOD/DEMOD OF TRANSDUCER SIGNALS**
- **PRECISION LONG TERM INTEGRATOR**
- **HIGH RESOLUTION OPTICAL LINK FOR ISOLATION**
- **AC LINE FREQUENCY MONITOR**
- **MOTOR SPEED MONITOR AND CONTROL**

### DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with  $-In$  and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up ( $f_{OUT}$  to  $+V_{CC}$ ). The VFC320 is available in three performance/temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ranges, and the dual-in-line units are specified from  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



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# SPECIFICATIONS

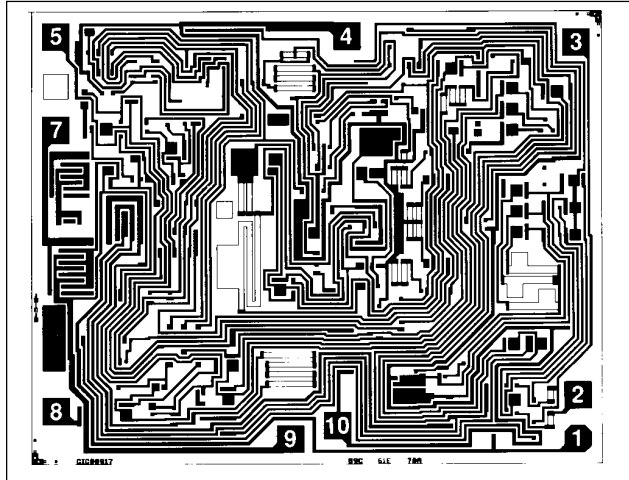
At  $T_A = +25^\circ\text{C}$  and  $\pm 15\text{VDC}$  power supply, unless otherwise noted.

PARAMETER	CONDITIONS	VFC320BG/BM/SM			VFC320CG/CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>V/F CONVERTER</b> $f_{\text{OUT}} = V_{\text{IN}}/7.5 R_1 C_1$ , Figure 4								
<b>INPUT TO OP AMP</b> Voltage Range <sup>(1)</sup> Current Range <sup>(1)</sup> Bias Current Inverting Input Noninverting Input Offset Voltage <sup>(3)</sup> Offset Voltage Drift Differential Impedance Common-Mode Impedance	Fig. 4 with $e_2 = 0$ Fig. 4 with $e_1 = 0$ $I_{\text{IN}} = V_{\text{IN}}/R_{\text{IN}}$	>0 <0 +0.25		Note 2 -10 +750				V V $\mu\text{A}$ nA nA mV $\mu\text{V}/^\circ\text{C}$ $\text{k}\Omega \parallel \text{pF}$ $\text{k}\Omega \parallel \text{pF}$
<b>ACCURACY</b> Linearity Error <sup>(1) (4) (5)</sup>  Offset Error Input Offset Voltage <sup>(3)</sup> Offset Drift <sup>(7)</sup> Gain Error <sup>(3)</sup> Gain Drift <sup>(7)</sup> Full Scale Drift (Offset Drift and Gain Drift) <sup>(7)(8)(9)</sup> Power Supply Sensitivity	Fig. 4 with $e_2 = 0$ <sup>(6)</sup> $0.01\text{Hz} \leq f_{\text{OUT}} \leq 10\text{kHz}$ $0.1\text{Hz} \leq f_{\text{OUT}} \leq 100\text{kHz}$ $1\text{Hz} \leq f_{\text{OUT}} \leq 1\text{MHz}$  $f = 10\text{kHz}$ $f = 10\text{kHz}$  $\pm V_{\text{CC}} = 14\text{VDC to } 18\text{VDC}$			$\pm 0.004$ $\pm 0.008$ $\pm 0.1$  $\pm 15$ $\pm 0.5$ $\pm 5$  $\pm 0.015$ $\pm 0.002$ $\pm 0.002$  $\pm 0.015$				% FSR % FSR % FSR  ppm FSR ppm FSR/ $^\circ\text{C}$ % FSR ppm FSR/ $^\circ\text{C}$ ppm FSR/ $^\circ\text{C}$ % FSR%
<b>DYNAMIC RESPONSE</b> Full Scale Frequency Dynamic Range Settling Time  Overload Recovery	$C_{\text{LOAD}} \leq 50\text{pF}$  (V/F) to Specified Linearity For a Full Scale Input Step <50% Overload	6		1  Note 10 Note 10				MHz Decades  ns
<b>OPEN COLLECTOR OUTPUT</b> Voltage, Logic "0" Leakage Current, Logic "1" Voltage, Logic "1"  Duty Cycle at FS Fall Time	$I_{\text{SINK}} = 8\text{mA, max}$ $V_O = 15\text{V}$ External Pull-up Resistor Required (See Figure 4) For Best Linearity $I_{\text{OUT}} = 5\text{mA, } C_{\text{LOAD}} = 500\text{pF}$			0.4 1.0  $V_{\text{PU}}$ 25 100				V $\mu\text{A}$ V % ns
<b>F/V CONVERTER</b> $V_{\text{OUT}} = 7.5 R_1 C_1 f_{\text{IN}}$ , Figure 9								
<b>INPUT TO COMPARATOR</b> Impedance Logic "1" Logic "0" Pulse-width Range		50 $\parallel$ 10 +1.0 - $V_{\text{CC}}$ 0.25	150 $\parallel$ 10	$+V_{\text{CC}}$ -0.05				$\text{k}\Omega \parallel \text{pF}$ V V $\mu\text{s}$
<b>OUTPUT FROM OP AMP</b> Voltage Current Impedance Capacitive Load	$I_O = 6\text{mA}$ $V_O = 7\text{VDC}$ Closed-Loop Without Oscillation	0 to +10 +10		0.1 100				V mA $\Omega$ pF
<b>POWER SUPPLY</b> Rated Voltage Voltage Range Quiescent Current		$\pm 13$	$\pm 15$	$\pm 20$ $\pm 7.5$				V V mA
<b>TEMPERATURE RANGE</b> Specification B and C Grades S Grade Operating B and C Grades S Grade Storage		-25 -55		+85 +125				$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$

\* Specification the same as for VFC320BG/BM/SM.

NOTES: (1) A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity. (2) Determined by  $R_{\text{IN}}$  and full scale current range constraints. (3) Adjustable to zero. See Offset and Gain Adjustment section. (4) Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. (5) When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy. (6) For  $e_1 = 0$  typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz. (7) Exclusive of external components' drift. (8) FSR = Full Scale Range (corresponds to full scale and full scale input voltage.) (9) Positive drift is defined to be increasing frequency with increasing temperature. (10) One pulse of new frequency plus 50ns typical.

## DICE INFORMATION



VFC320 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	$V_{OUT}$ (Int. Out)	6	NC
2	+In	7	$f_{OUT}$
3	-In	8	Comp. Input
4	$-V_{CC}$	9	Common
5	One-Shot Cap.	10	$+V_{CC}$

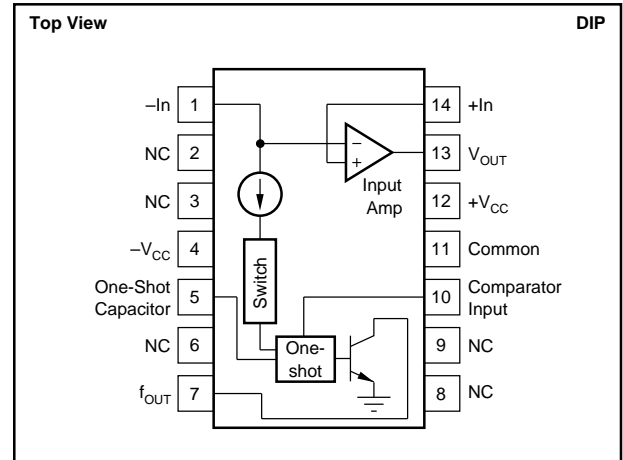
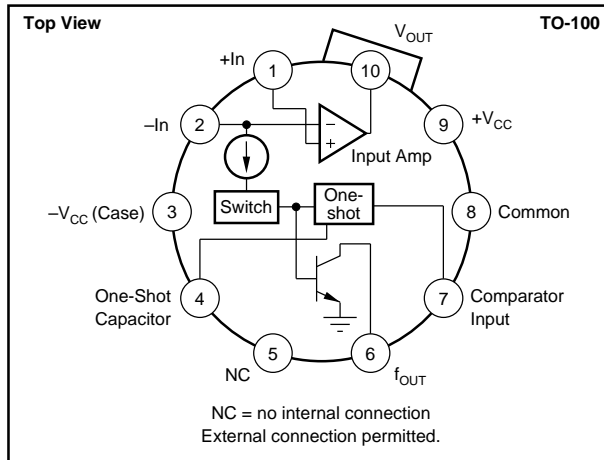
NC: No Connection.

Substrate Bias: Electrically connected to  $-V_s$  supply.

## MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	109 x 87 ±5	2.77 x 2.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	

## CONNECTION DIAGRAM



## ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
VFC320BG	14-Pin Ceramic DIP	-25°C to +85°C
VFC320BM	TO-100	-25°C to +85°C
VFC320SM	TO-100	-55°C to +125°C
VFC320CG	14-Pin Ceramic DIP	-25°C to +85°C
VFC320CM	TO-100	-25°C to +85°C

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Output Sink Current at $f_{OUT}$	50mA
Output Current at $V_{OUT}$	+20mA
Input Voltage, -Input	± $V_{CC}$
Input Voltage, +Input	± $V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
VFC320BG	14-Pin Ceramic DIP	163
VFC320BM	TO-100	007
VFC320SM	TO-100	007
VFC320CG	14-Pin Ceramic DIP	163
VFC320CM	TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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# DISCUSSION OF SPECIFICATIONS

## LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero.) Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ( $\Delta f_{OUT}/\Delta V_{IN}$ ) with operation as close to the chosen full scale frequency as possible. The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission.)

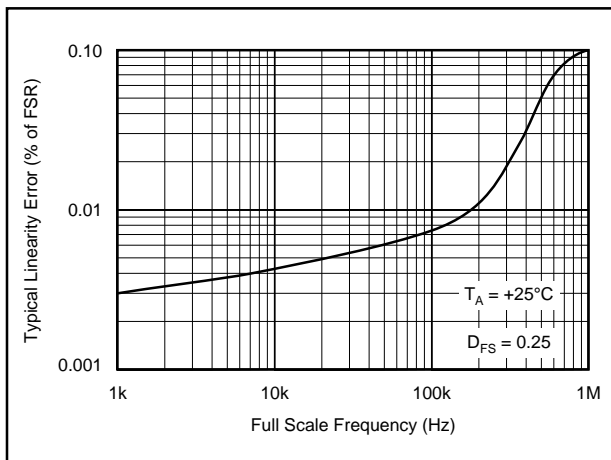


Figure 1. Linearity Error vs Full Scale Frequency.

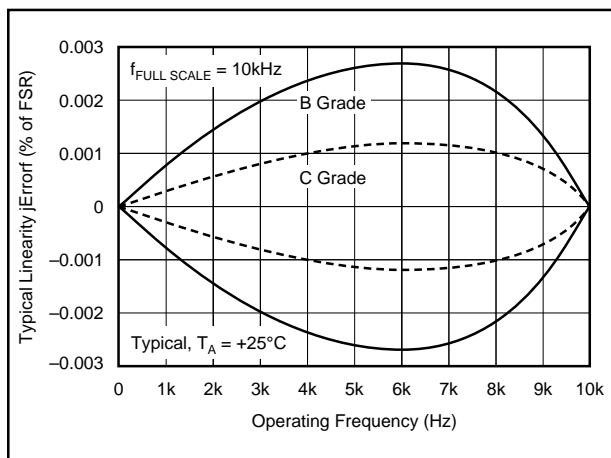


Figure 2. Linearity Error vs Operating Frequency.

## FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially  $R_1$  and  $C_1$ ) must be added to the drift of the VFC320.

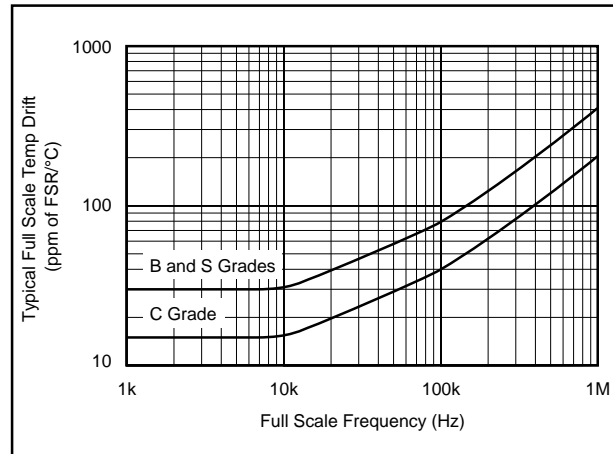


Figure 3. Full Scale Drift vs Full Scale Frequency.

## RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50ns plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within  $\pm 0.01\%$  of full scale is 10 $\mu$ s.

## THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a on-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at  $V_{IN}$ , a current will flow through the input resistor, causing the voltage at  $V_{OUT}$  to ramp down toward zero, according to  $dV/dt = V_{IN}/R_1C_1$ . During this time the constant current sink is disabled by the switch. Note, this period is only dependent on  $V_{IN}$  and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing  $f_{OUT}$  from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through  $C_1$  until  $V_{C1} = -7.5V$ . Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this  $-7.5V$  threshold point  $C_1$ , comparator B resets the flip-flop, and the ramp voltage

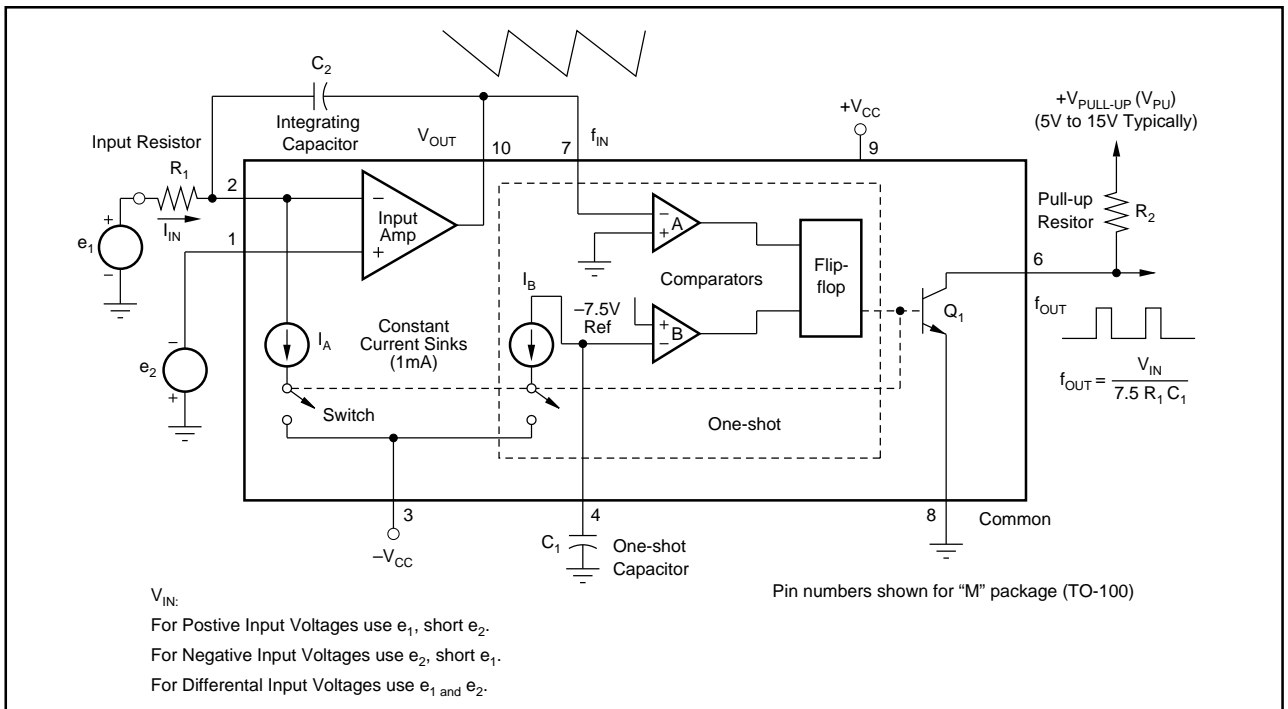


FIGURE 4. Functional Block Diagram of the VFC320.

begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor,  $C_1$ . After the one-shot resets,  $f_{OUT}$  changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

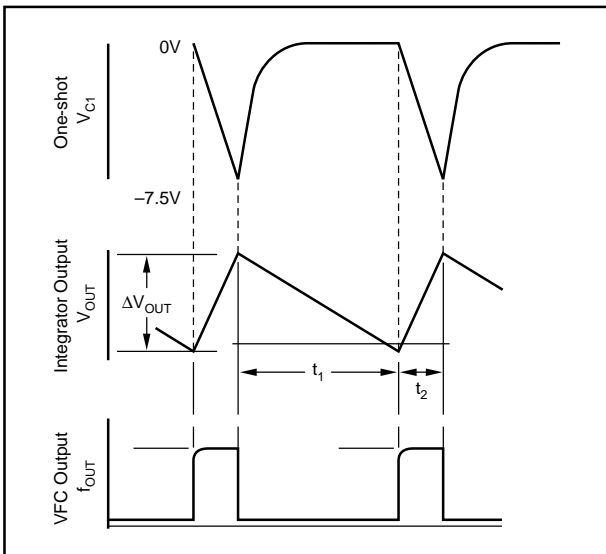


FIGURE 5. Integrator and VFC Output Timing.

In the time  $t_1 + t_2$  the integrator capacitor  $C_2$  charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN} t_1 + (I_{IN} - I_A) t_2 \quad (2)$$

$$\text{So that } I_{IN} (t_1 + t_2) = I_A t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_2 R_2} \quad (6)$$

In the time  $t_1$ ,  $I_B$  charges the one-shot capacitor  $C_1$  until its voltage reaches  $-7.5V$  and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

Since  $I_A = I_B$  the result is

$$f_{OUT} = \frac{V_{IN}}{7.5 R_1 C_1} \quad (9)$$

Since the integrating capacitor,  $C_2$ , affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to  $I_{IN}$ , since this parameter will add directly to the gain error of the VFC.  $C_1$ , which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter.  $e_1$  and  $e_2$  are shorted and  $F_{IN}$  is disconnected from  $V_{OUT}$ .  $F_{IN}$  is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by  $C_1$  as before, but the cycle repetition frequency will be dictated by the digital input at  $F_{IN}$ .

### DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period ( $t_2$ ) or pulse width, PW, to the total VFC period ( $t_1 + t_2$ ). For the VFC320,  $t_2$  is fixed and  $t_1 + t_2$  varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency,  $D_{FS}$ , which occurs at full scale input.  $D_{FS}$  is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when  $D_{FS}$  is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN\ max} / R_1}{1\text{mA}} = \frac{I_{IN\ max}}{1\text{mA}}$$

Thus  $D_{FS} = 0.25$  corresponds to  $I_{IN\ max} = 0.25\text{mA}$ .

## INSTALLATION AND OPERATING INSTRUCTIONS

### VOLTAGE-TO-FREQUENCY CONVERSION

The VCF320 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

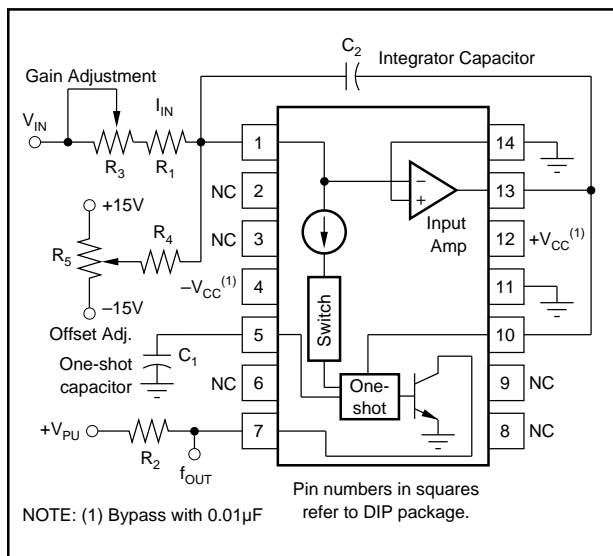


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

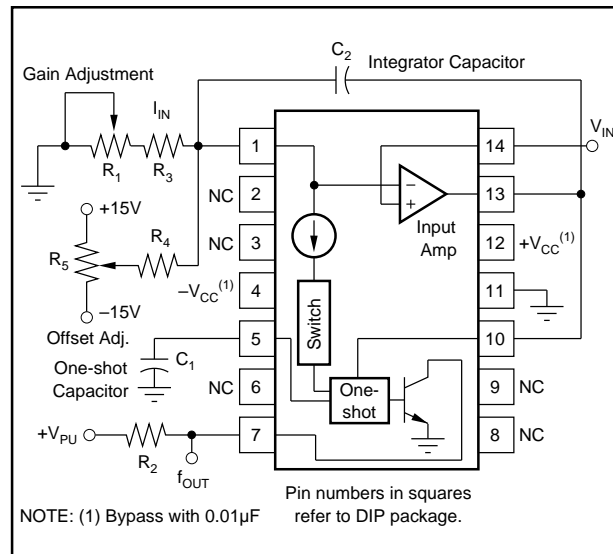


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

### EXTERNAL COMPONENT SELECTION

In general, the design sequence consists of: (1) choosing  $f_{MAX}$ , (2) choosing the duty cycle at full scale ( $D_{FS} = 0.25$  typically), (3) determining the input resistor,  $R_1$  (Figure 4), (4) calculating the one-shot capacitor,  $C_1$ , (5) selecting the integrator capacitor  $C_2$ , and (6) selecting the output pull-up resistor,  $R_2$ .

#### Input Resistors $R_1$ and $R_3$

The input resistance ( $R_1$  and  $R_3$  in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than  $D_{FS} = 0.25$  may be used but linearity will be affected.

The nominal value is  $R_1$  is

$$R_1 = \frac{V_{IN\ max}}{0.25\text{mA}} \quad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of  $C_1$  and the desired trim range.  $R_1$  should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

#### One-Shot Capacitor, $C_1$

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_1\ \text{NOM} = \frac{V_{IN}}{7.5 R_1 f_{OUT}} \quad (11)$$

For the usual 25% duty at  $f_{MAX} = V_{IN}/R_1 = 0.25\text{mA}$  there is approximately 15pF of residual capacitance so that the design value is

$$C_1(\text{pF}) = \frac{33 \times 10^6}{f_{FS}} - 15 \quad (12)$$

where  $f_{FS}$  is the full scale output frequency in Hz. The temperature drift of  $C_1$  is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with  $C_1$ . It should be mounted as close to the VFC320 as possible. Figure 8 shows pulse width and full scale frequency for various values of  $C_1$  at  $D_{FS} = 25\%$ .

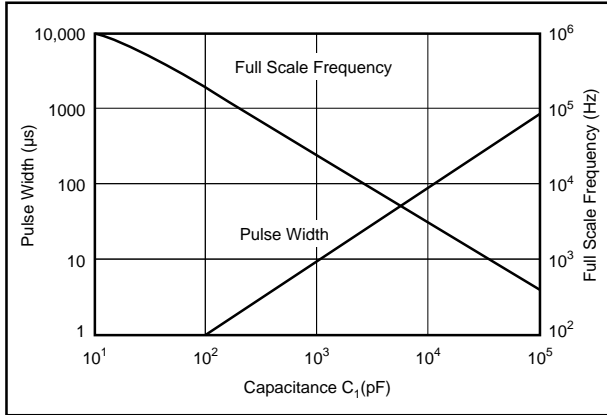


FIGURE 8. Output Pulse Width ( $D_{FS} = 0.25$ ) and Full Scale Frequency vs External One-shot Capacitance.

### Integrating Capacitor, $C_2$

Since  $C_2$  does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in  $C_2$  causes a gain error. A ceramic type is sufficient for most applications. The value of  $C_2$  determines the amplitude of  $V_{OUT}$ . Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator determine a range of acceptable values,

$$C_2 (\mu\text{F}) = \begin{cases} 100/f_{FS}; & \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001; & \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005; & \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

### Output Pull Up Resistor $R_2$

The open collector output can sink up to 8mA and still be TTL-compatible. Select  $R_2$  according to this equation:

$$R_2 \text{ min } (\Omega) = V_{PULLUP} / (8\text{mA} - I_{LOAD})$$

A 10% carbon film resistor is suitable for use as  $R_2$ .

### Trimming Components $R_3$ , $R_4$ , $R_5$

$R_5$  nulls the offset voltage of the input amplifier. It should have a series resistance between 10k $\Omega$  and 100k $\Omega$  and a temperature coefficient less than 100ppm/ $^{\circ}\text{C}$ .  $R_4$  can be a 10% carbon film resistor with a value of 10M $\Omega$ .

$R_3$  nulls the gain errors of the converter and compensates for initial tolerances of  $R_1$  and  $C_1$ . Its total resistance should be at least 20% of  $R_1$ , if  $R_1$  is selected 10% low. Its temperature coefficient should be no greater than five times that of  $R_1$  to maintain a low drift of the  $R_3 - R_1$  series combination.

## OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust  $R_5$  for proper output.
3. Apply the full scale input voltage.
4. Adjust  $R_3$  for proper output.
5. Repeat stems 1 through 4.

If nulling is unnecessary for the application, delete  $R_4$  and  $R_5$ , and replace  $R_3$  with a short circuit.

## POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC320 is 0.015% of FSR/% max. To maintain  $\pm 0.015\%$  conversion, power supplies which are stable to within  $\pm 1\%$  are recommended. These supplies should be bypassed as close as possible to the converter with 0.01 $\mu\text{F}$  capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the  $f_{OUT}$  pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

## DESIGN EXAMPLE

Given a full scale input of +10V, select the values of  $R_1$ ,  $R_2$ ,  $R_3$ ,  $C_1$ , and  $C_2$  for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

### Selecting $C_1$ ( $D_{FS} = 0.25$ )

$$C_1 = [(33 \times 10^6) / f_{MAX}] - 15 \quad [(66 \times 10^6) / f_{MAX}] - 15 \\ \text{if } D_{FS} = 0.5 \\ = [(33 \times 10^6) / 100\text{kHz}] - 15 \\ = 315\text{pF}$$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

### Selecting $R_1$ and $R_3$ ( $D_{RS} = 0.25$ )

$$R_1 + R_3 = V_{IN \text{ max}} / 0.25\text{mA} \quad V_{IN \text{ max}} / 0.5\text{mA} \\ \text{if } D_{FS} = 0.5 \\ = 10\text{V} / 0.25\text{mA} \\ = 40\text{k}\Omega$$

Choose 32.4k $\Omega$  metal film resistor with 1% tolerance and  $R_3 = 10\text{k}\Omega$  cermet potentiometer.

### Selecting $C_2$

$$C_2 = 10^2 / F_{MAX} \\ = 10^2 / 100\text{kHz} \\ = 0.001\mu\text{F}$$

Choose a 0.001 $\mu\text{F}$  capacitor with  $\pm 5\%$  tolerance.

## Selecting R<sub>2</sub>

$$R_2 = V_{PULLUP} / (8\text{mA} - I_{LOAD})$$

$$= 5\text{V} / (8\text{mA} - 1.6\text{mA}), \text{ one TTL-load} = 1.6\text{mA}$$

$$= 781\Omega$$

Choose a 750Ω 1/4-watt carbon compensation resistor with ±5% tolerance.

pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold.

Errors are nulled using 0.001 X full scale frequency to null offset, and full scale frequency to null the gain error. The procedure is given on this page. Use equations from V/F calculations to find R<sub>1</sub>, R<sub>3</sub>, R<sub>4</sub>, C<sub>1</sub> and C<sub>2</sub>.

## FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC320 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C<sub>3</sub> to make  $t = 0.1t$  (see Figure 9). For input signals with amplitudes less than 5V,

## TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits

Figures 10-14 show typical applications of the VFC320.

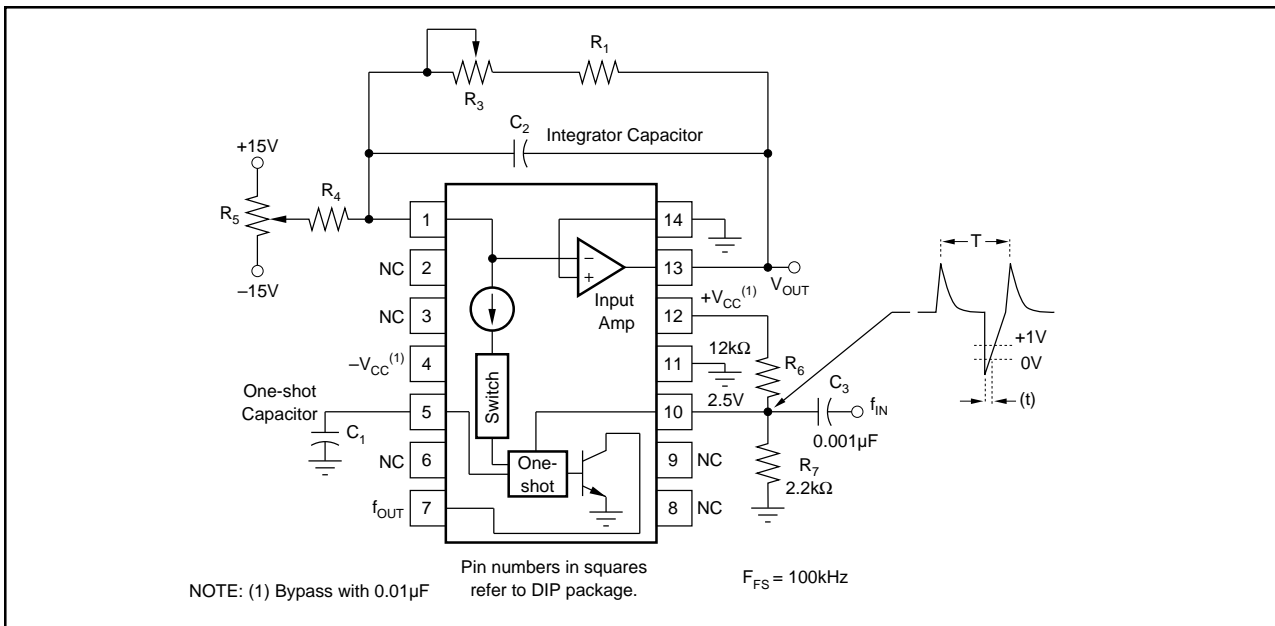


FIGURE 9. Connection Diagram for F/V Conversion.

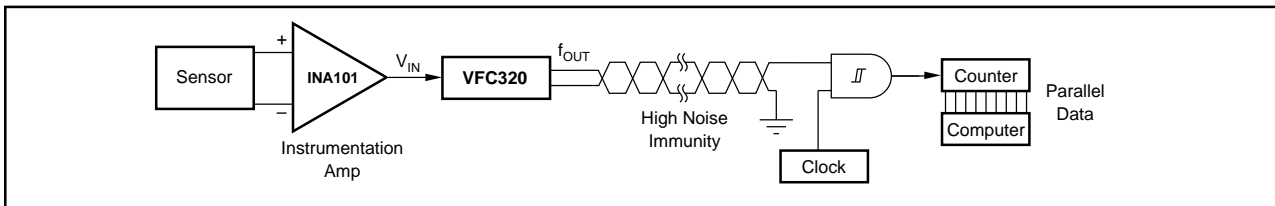


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

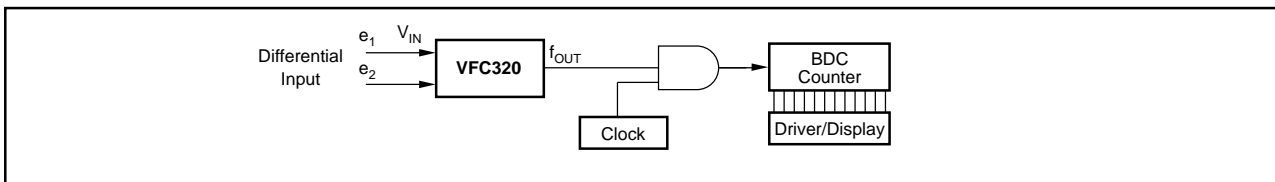


FIGURE 11. Inexpensive Digital Panel Meter.



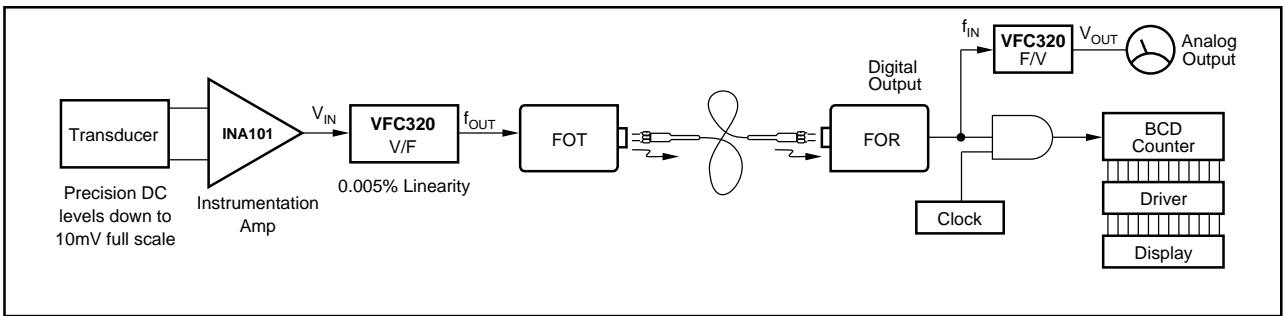


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (Analog and Digital Output).

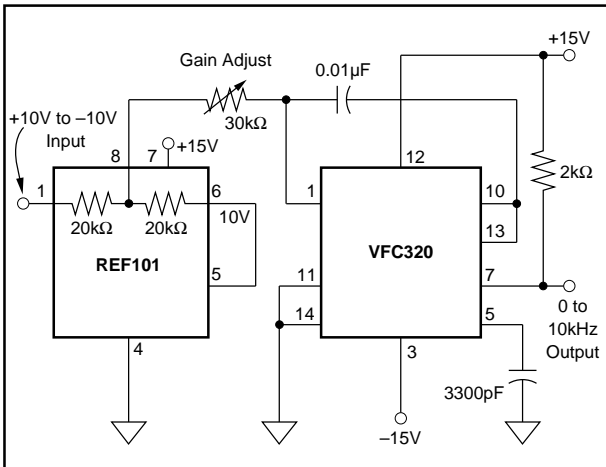


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

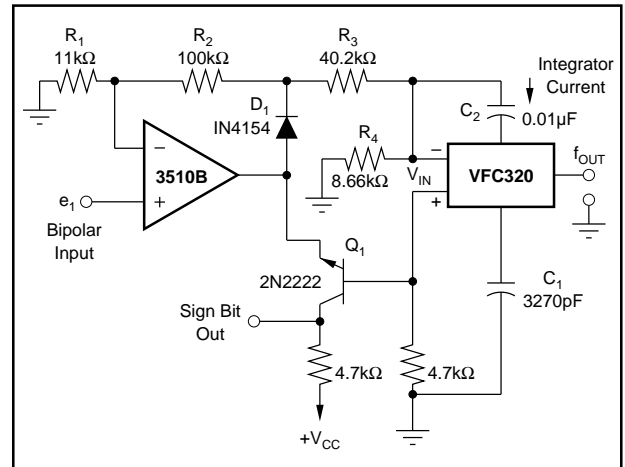


FIGURE 14. Absolute value circuit with the VFC320. Op amp,  $D_1$  and  $Q_1$  (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to  $|e_1|$ . The sign bit output provides indication of the input polarity.